Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	wan same (edge adj witch) same ports	USPAT	OR	ON	2005/02/05 17:30
L2	0	(wan or (wide adj area adj network))same (edge adj witch) same ports	USPAT	OR	ON	2005/02/05 17:30
L3	0	(wan or (wide adj area adj network)) and (edge adj witch) same ports	USPAT	OR	ON	2005/02/05 17:31
L4	10	(wan or (wide adj area adj network)) and (edge adj switch) same ports	USPAT	OR	ON	2005/02/05 17:31
L5	0	(wan or (wide adj area adj network))same(edge adj switch) same ports	USPAT	OR	ON	2005/02/05 17:31
L6	10	(wan or (wide adj area adj network))and (edge adj switch) same ports	USPAT	OR	ON	2005/02/05 17:31
L7	10	(wan or (wide adj area adj network))and (edge adj switch$4) same ports	USPAT	OR	ON	2005/02/05 17:32
L8	1	(wan or (wide adj area adj network))and (edge adj switch$4) same ports and 709/2$$.ccls.	USPAT	OR	ON	2005/02/05 17:35
L9	6	(wan or (wide adj area adj network))and (edge adj switch$4) same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:35
L10	60	(wan or (wide adj area adj network))and (switch$4 adj device) same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:42
L11	0	(wan or (wide adj area adj network))and (switch$4 adj device) same ports and bridge$2 and 709/ccls.	USPAT	OR	ON	2005/02/05 17:37
L12	9	(wan or (wide adj area adj network))and (switch$4 adj device) same ports and bridge$2 and 709/2$$.ccls.	USPAT	OR	ON	2005/02/05 17:41
L13	3	(wan or (wide adj area adj network))and (switch$4 adj devices) same ports and bridge$2 and 709/2$$.ccls.	USPAT	OR	ON	2005/02/05 17:42
L14	3	(wan or (wide adj area adj network))and (switch$3 adj devices) same ports and bridge$2 and 709/2$$.ccls.	USPAT	OR	ON	2005/02/05 17:42

L15	0	(wan or (wide adj area adj network))and (eadge adj switches) same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:43
L16	865	(wan or (wide adj area adj network))and switches same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:43
L17	142	(wan or (wide adj area adj network))same switches same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:43
L18	40	(wan or (wide adj area adj network))with switches same ports and bridge$2	USPAT	OR	ON	2005/02/05 17:43
L19	16	(wan or (wide adj area adj network))with switches same ports same bridge$2	USPAT	OR	ON	2005/02/05 17:43
L20	7	(wan or (wide adj area adj network))with switches same ports same bridge$2 and 709/2$$.ccls.	USPAT	OR	ON	2005/02/05 17:47
L21	15	(wan or (wide adj area adj network))with switches same ports same bridge$2 and state	USPAT	OR	ON	2005/02/05 17:47
L22	15	(wan or (wide adj area adj network))with switches same ports same bridge$2 and states	USPAT	OR	ON	2005/02/05 17:48
L23	7	(wan or (wide adj area adj network))with switches same ports same bridge$2 and active and block same states	USPAT	OR	ON	2005/02/05 17:49
L24	1	(wan or (wide adj area adj network))with switches same ports same bridge$2 and (active adj states)	USPAT	OR	ON	2005/02/05 17:49
L25	1	(wan or (wide adj area adj network))with switches same ports same bridge$2 and (active adj states) and block$4	USPAT	OR	ON	2005/02/05 17:50
L26	22	(wan or (wide adj area adj network)) same switches same ports and bridge$2 and (active adj states) and block$4	USPAT	OR	ON	2005/02/05 17:50
L27	21	(wan or (wide adj area adj network)) same switches same ports same bridge$2 and (active adj states) and block$4	USPAT	OR	ON	2005/02/05 17:53
L28	0	(wan or (wide adj area adj network)) same switches same ports same bridge$2 and (active adj states) and (block$4 adj state)	USPAT	OR	ON	2005/02/05 17:54

Your search matched **3** of **1123491** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enterin new one in the text box.

switches<and>ports<and>state<and> active<and>block Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **A 100-MHz 8-mW ROM-less quadrature direct digital frequency synthesizer**
Mohieldin, A.N.; Emira, A.A.; Sanchez-Sinencio, E.;
Solid-State Circuits, IEEE Journal of , Volume: 37 , Issue: 10 , Oct. 2002
Pages:1235 - 1243

[Abstract] [PDF Full-Text (432 KB)] **IEEE JNL**

---

2 **Simple hybrid systems for accurate synthesis and analysis of harmo spectra**
Scott, S.; Stromberg, H.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '76. , Volume: 1 , Apr 1976
Pages:630 - 632

[Abstract] [PDF Full-Text (68 KB)] **IEEE CNF**

---

3 **A reconfigurable DMOS control chip for an electronic typewriter**
Pietrobon, G.; Rossi, D.;
Solid-State Circuits Conference, 1989. Digest of Technical Papers. 36th ISSCC 1989 IEEE International , 15-17 Feb. 1989
Pages:200 - 201, 342

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

Terms used
switches and **change** and **state** and **ports** and **block** and **active**

Found **84,913** of **150,138**

Sort results by relevance

Display results expanded form

Save results to a Binder

Search Tips

☐ Open results in a new window

Try an Advanced Search

Try this search in The ACM Guide

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next

Best 200 shown

Relevance scale

1 Fast detection of communication patterns in distributed executions

Thomas Kunz, Michiel F. H. Seuren

November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

2 Dynamic queue length thresholds for shared-memory packet switches

Abhijit K. Choudhury, Ellen L. Hahne

April 1998 **IEEE/ACM Transactions on Networking (TON)**, Volume 6 Issue 2

Full text available: pdf(324.50 KB) Additional Information: full citation, references, citings, index terms

Keywords: adaptive thresholds, asynchronous transfer mode, buffer allocation, dynamic thresholds, memory management, pushout, queue length thresholds, shared-memory switch

3 Performance counters and state sharing annotations: a unified approach to thread locality

Boris Weissman

October 1998 **Proceedings of the eighth international conference on Architectural support for programming languages and operating systems**, Volume 33 , 32 Issue 11 , 5

Full text available: pdf(1.76 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a combined approach for improving thread locality that uses the bardware performance monitors of modem processors and program-centric code annotations to guide thread scheduling on SMPs. The approach relies on a shared state cache model to compute expected thread footprints in the cache on-line. The accuracy of the

model has been analyzed by simmations involving a set of parallel applications. We demonstrate how the cache model can be used to implement several practical loca ...

4 Power minimization in IC design: principles and applications

Massoud Pedram
January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

5 BrouHaHa- A portable Smalltalk interpreter

Eliot Miranda
December 1987 **ACM SIGPLAN Notices , Conference proceedings on Object-oriented programming systems, languages and applications**, Volume 22 Issue 12

Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

BrouHaHa is a portable implementation of the Smalltalk-80 virtual machine interpreter. It is a more efficient redesign of the standard Smalltalk specification, and is tailored to suit conventional 32 bit microprocessors. This paper presents the major design changes and optimization techniques used in the BrouHaHa interpreter. The interpreter runs at 30% of the speed of the Dorado on a Sun 3/160 workstation. The implementation is portable because it is written in C.

6 Balancing performance and flexibility with hardware support for network architectures

Ilija Hadžić, Jonathan M. Smith
November 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 4

Full text available: pdf(719.03 KB) Additional Information: full citation, abstract, references, index terms

The goals of performance and flexibility are often at odds in the design of network systems. The tension is common enough to justify an architectural solution, rather than a set of context-specific solutions. The Programmable Protocol Processing Pipeline (P4) design uses programmable hardware to selectively accelerate protocol processing functions. A set of field-programmable gate arrays (FPGAs) and an associated library of network processing modules implemented in hardware are augmented with so ...

Keywords: FPGA, P4, computer networking, flexibility, hardware, performance, programmable logic devices, programmable networks, protocol processing

7 Low-energy off-chip SDRAM memory systems for embedded applications

Hojun Shim, Yongsoo Joo, Yongseok Choi, Hyung Gyu Lee, Naehyuck Chang

February 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 1

Full text available: pdf(3.98 MB) Additional Information: full citation, abstract, references, index terms

Memory systems are dominant energy consumers, and thus many energy reduction techniques for memory buses and devices have been proposed. For practical energy reduction practices, we have to take into account the interaction between a processor and cache memories together with application programs. Furthermore, energy characterization of memory systems must be accurate enough to justify various techniques. In this article, we build an in-house energy simulator for memory systems that is accelerat ...

Keywords: Low power, SDRAM, memory system

8 Reconfigurable computing: a survey of systems and software

Katherine Compton, Scott Hauck
June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2

Full text available: pdf(710.56 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single chip architectures to multi-chip systems, including internal structures and external coupling. W ...

Keywords: Automatic design, FPGA, field-programmable, manual design, reconfigurable architectures, reconfigurable computing, reconfigurable systems

9 Cache Memories

Alan Jay Smith
September 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 3

Full text available: pdf(4.61 MB) Additional Information: full citation, references, citings, index terms

10 The state of the art in locally distributed Web-server systems

Valeria Cardellini, Emiliano Casalicchio, Michele Colajanni, Philip S. Yu
June 2002 **ACM Computing Surveys (CSUR)**, Volume 34 Issue 2

Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, citings, index terms

The overall increase in traffic on the World Wide Web is augmenting user-perceived response times from popular Web sites, especially in conjunction with special events. System platforms that do not replicate information content cannot provide the needed scalability to handle large traffic volumes and to match rapid and dramatic changes in the number of clients. The need to improve the performance of Web-based services has produced a variety of novel content delivery architectures. This article w ...

Keywords: Client/server, World Wide Web, cluster-based architectures, dispatching algorithms, distributed systems, load balancing, routing mechanisms

11 Cache performance of operating system and multiprogramming workloads

Anant Agarwal, John Hennessy, Mark Horowitz

November 1988 **ACM Transactions on Computer Systems (TOCS)**, Volume 6 Issue 4

Full text available: pdf(3.16 MB) Additional Information: full citation, abstract, references, citings, index terms, review

Large caches are necessary in current high-performance computer systems to provide the required high memory bandwidth. Because a small decrease in cache performance can result in significant system performance degradation, accurately characterizing the performance of large caches is important. Although measurements on actual systems have shown that operating systems and multiprogramming can affect cache performance, previous studies have not focused on these effects. We have developed a pro ...

12 Draft Proposed: American National Standard—Graphical Kernel System

Technical Committee X3H3 - Computer Graphics
February 1984 **ACM SIGGRAPH Computer Graphics**, Volume 18 Issue SI

Full text available: pdf(16.07 MB) Additional Information: full citation

13 Dynamic queue length thresholds for multiple loss priorities

Ellen L. Hahne, Abhijit K. Choudhury
June 2002 **IEEE/ACM Transactions on Networking (TON)**, Volume 10 Issue 3

Full text available: pdf(545.38 KB) Additional Information: full citation, abstract, references, citings, index terms

Buffer management schemes are needed in shared-memory packet switches to regulate the sharing of memory among different output port queues and among traffic classes with different loss priorities. Earlier we proposed a single-priority scheme called Dynamic Threshold (DT), in which the maximum permissible queue length is proportional to the unused buffering in the switch. A queue whose length equals or exceeds the current threshold value may accept no new arrivals. In this paper, we propose, anal ...

Keywords: buffer management, congestion control, loss priorities, packet switching, queue length thresholds, selective discarding, shared memory, space priorities

14 Security Mechanisms in High-Level Network Protocols

Victor L. Voydock, Stephen T. Kent
June 1983 **ACM Computing Surveys (CSUR)**, Volume 15 Issue 2

Full text available: pdf(3.23 MB) Additional Information: full citation, references, citings

15 Run-time adaptation in river

Remzi H. Arpaci-Dusseau
February 2003 **ACM Transactions on Computer Systems (TOCS)**, Volume 21 Issue 1

Full text available: pdf(849.04 KB) Additional Information: full citation, abstract, references, index terms

We present the design, implementation, and evaluation of run-time adaptation within the River dataflow programming environment. The goal of the River system is to provide adaptive mechanisms that allow database query-processing applications to cope with performance variations that are common in cluster platforms. We describe the system and its basic mechanisms, and carefully evaluate those mechanisms and their effectiveness. In our analysis, we answer four previously unanswered and important que ...

Keywords: Performance availability, clusters, parallel I/O, performance faults, robust performance, run-time adaptation

16 Pen computing: a technology overview and a vision

André Meyer
July 1995 **ACM SIGCHI Bulletin**, Volume 27 Issue 3

Full text available: pdf(5.14 MB) Additional Information: full citation, abstract, citings, index terms

This work gives an overview of a new technology that is attracting growing interest in public as well as in the computer industry itself. The visible difference from other technologies is in the use of a pen or pencil as the primary means of interaction between a user and a machine, picking up the familiar pen and paper interface metaphor. From this follows a set of consequences that will be analyzed and put into context with other emerging technologies and visions.Starting with a short historic ...

17 Experience Using Multiprocessor Systems—A Status Report

Anita K. Jones, Peter Schwarz
June 1980 **ACM Computing Surveys (CSUR)**, Volume 12 Issue 2

Full text available: pdf(4.48 MB) Additional Information: full citation, references, citings, index terms

18 The embedded machine: predictable, portable real-time code

Thomas A. Henzinger, Christoph M. Kirsch
May 2002 **ACM SIGPLAN Notices , Proceedings of the ACM SIGPLAN 2002 Conference on Programming language design and implementation**, Volume 37 Issue 5

Full text available: pdf(223.85 KB) Additional Information: full citation, abstract, references, citings, index terms

The Embedded Machine is a virtual machine that mediates in real time the interaction between software processes and physical processes. It separates the compilation of embedded programs into two phases. The first, platform-independent compiler phase generates E code (code executed by the Embedded Machine), which supervises the timing ---not the scheduling--- of application tasks relative to external events, such as clock ticks and sensor interrupts. E~code is portable and exhibits, given an inpu ...

Keywords: real time, virtual machine

19 Concepts and Notations for Concurrent Programming

Gregory R. Andrews, Fred B. Schneider
January 1983 **ACM Computing Surveys (CSUR)**, Volume 15 Issue 1

Full text available: pdf(4.02 MB) Additional Information: full citation, references, citings, index terms

20 System-level power optimization: techniques and tools

Luca Benini, Giovanni de Micheli
April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 5 Issue 2

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods